Design and Layout Implementation of an 8-to-1 Multiplexer Using 0.12 µm CMOS Technology

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Abstract

Multiplexer is one of the most essential components used to build Configurable Logic Blocks (CLBs) in Field Programmable Logic Arrays (FPGAs). In this paper, we present the design and analysis of an 8-to-1 multiplexer using 0.12 deep submicron CMOS technology. The 8-to-1 multiplexer is built by interconnecting two 4-to-1 multiplexers with one 2-to-1 multiplexer. In order to allow the output to give a full voltage swing from 0 V to V_{DD}, both 4-to-1 multiplexers and 2-to-1 multiplexer are constructed using CMOS transmission gates. The transistor level and layout simulations have been successfully validated. In comparison to the static combinational CMOS logic design, this method can certainly reduce the number of transistors implemented in the design, optimizing the design of multiplexers in the die.

Keywords- Configurable Logic Blocks, Field Programmable Logic Arrays, CMOS, Transmission Gates.

I. Introduction

Ever since the advent of VLSI technology [1 – 5], Application Specific Integrated Circuit (ASIC) devices have been made possible with the aid of Electronic Design Automation (EDA) tools. An ASIC is a chip designed to perform a specific function in a particular application. In order to optimize the cost and time to market, special architectures have been developed for ASIC designs. Among these architectures, Field Programmable Gate Arrays (FPGAs) are presently the most popular architecture used in the Integrated Circuit (IC) industries. An FPGA consists of arrays of Configurable Logic Blocks (CLBs) which can be programmed to implement any logic functions of its inputs [1]. Hence, the FPGA can easily be configured by simply downloading configuration bits that program functions into the CLBs and properly interconnecting the arrays of CLBs. Multiplexer based logic has been extensively used to build CLBs [2]. A register which stores the output of a desired logic function is typically connected to the input of the multiplexer. Selection switches in the multiplexer determine which appropriate input signal from the register is to be sent to the output pin of the multiplexer [1, 2]. In this paper, we present the design and analysis of an 8-to-1 multiplexer commonly used in CLBs, using Microwind EDA tools. In order to allow full signal swing from 0 V to V_{DD}, we have implemented CMOS transmission gate configuration to construct the multiplexer. Here, the feature length (2λ) of both PMOS and NMOS is 0.12 µm.

II. Design

A 2-to-1 multiplexer is the fundamental building block for multiplexers with more than one selection switch and more than two input signals [1, 2]. Figs. 1 and 2 show the transistor level schematics of a 2-to-1 multiplexer and a 4-to-1 multiplexer respectively. As can be clearly seen, the 4-to-1 multiplexer is but merely the combination of three 2-to-1 multiplexers.

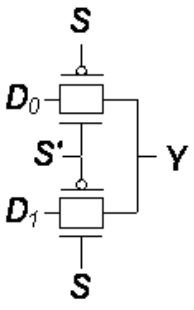

Fig. 1 A 2-to-1 multiplexer.

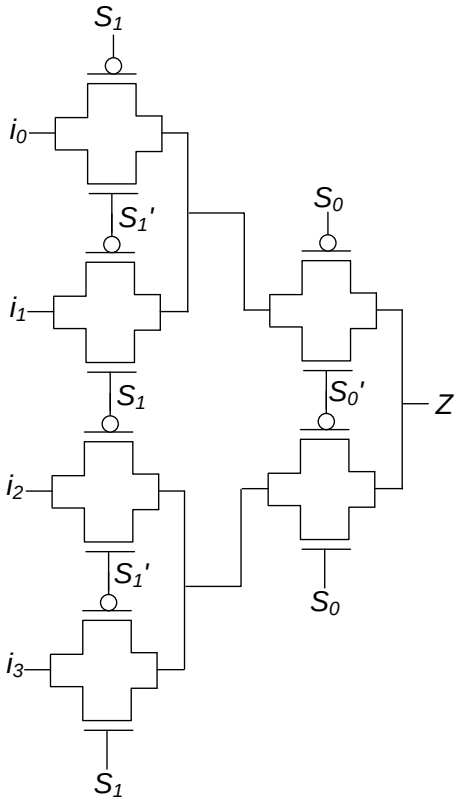

Fig. 2 A 4-to-1 multiplexer.

As illustrated in [1] and [2], two 4-to-1 multiplexers have been interconnected with a 2-to-1 multiplexer, for the case of an 8-to-1 multiplexer. As graphically depicted in Fig. 3, a total of seven 2-to-1 multiplexers have been used in the design.

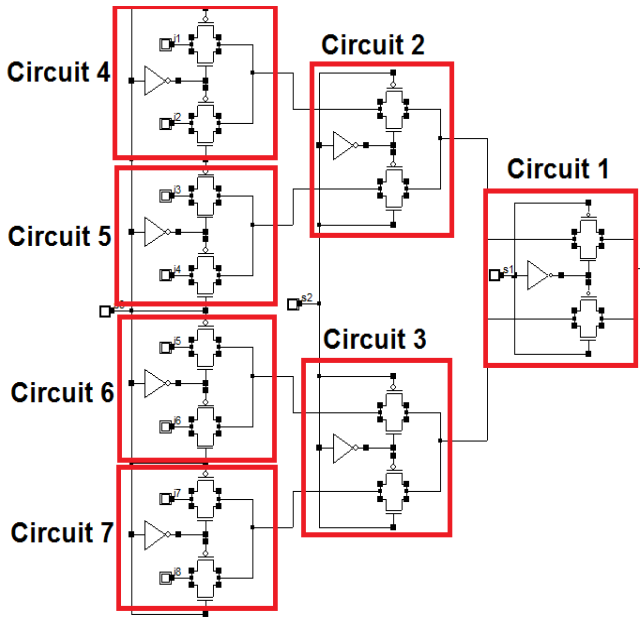

Fig. 3 An 8-to-1 multiplexer.

In order to illustrate the operational concept of the 8-to-1 multiplexer with ease, we have divided and labeled each 2-to-1 multiplexer as circuits 1 to 7, as shown in Fig. 3. The selection switch s_1 in circuit 1 determines either the multiplexers in circuit 2 or circuit 3 is to be activated. When a logic 1 (i.e. V_{DD}) is being supplied to s_1, circuit 3 will be activated; and vice versa, if a logic 0 is being supplied, circuit 2 will be activated instead. Subsequently, the selection switch s_2 of the multiplexer in circuit 2 is then used to control the activation of either circuit 4 or 5 in a similar manner. Likewise, the selection switch s_2 of the multiplexer in circuit 3 is used to determine either circuit 6 or 7 is to be activated. Table I depicts a summary of the output signal in correspond to different combination of selection switches.

III. Results and Discussion

As soon as the transistor level schematic has been validated, the layout of the 8-to-1 multiplexer is then generated using Microwind EDA tools, as shown in Fig. 4. In order to verify the design, clock pulses with different frequency rates have been inserted to the inputs i_1 to i_8, as well as, selection switches s_1 to s_3. Figs. 5 to 7 illustrate the timing diagrams of the input (i.e. i_1 to i_8 and s_1 to s_3) and output (i.e. *pmos_6_out1*) signals. As can be observed from Fig. 5, at time range 82 to 83 ns, 86 to 87 ns, 90 to 91 ns, and 94 to 95 ns, the output pin *pmos_6_out1* displays a logic 1 signal. At these time range, the selection switches $s_1s_2s_3$ = 100. Based on Table I, the multiplexer allows the input signal i_5 to be transmitted to the output. Comparison between the signals in both i_5 and *pmos_6_out1* shows that they agree very well (i.e. both are displaying a high signal in the diagram). At time range, 89 to 90 ns, 91 to 92 ns, 93 to 94 ns, and 95 to 96 ns, the selection switches $s_1s_2s_3$ = 110. From Table I, it can be clearly seen that the output signal should correspond to that supplied by input i_7. Clearly, both i_7 and *pmos_6_out1* tally very well, i.e. both displaying high signals in the timing diagram as well. Similarly, by performing close analysis on Figs. 6 and 7, it could be observed that when the selection switches $s_1s_2s_3$ = 010 and 001, respectively, the output signals agree very well with those shown in i_3 and i_1 as well. The results correspond with the desired outcomes summarized in Table I, verifying the validity of the design. In comparison to the static combinational CMOS logic

method [3], it is worthwhile noting that designing multiplexers using this method reduces the number of transistors implemented in the design significantly. This will certainly optimize the number of transistors in the die, allowing more functionalities to be incorporated into the die.

TABLE I

Truth table of an 8-to-1 multiplexer

$S_1S_2S_3$	Output
000	i_1
001	i_2
010	i_3
011	i_4
100	i_5
101	i_6
110	i_7
111	i_8

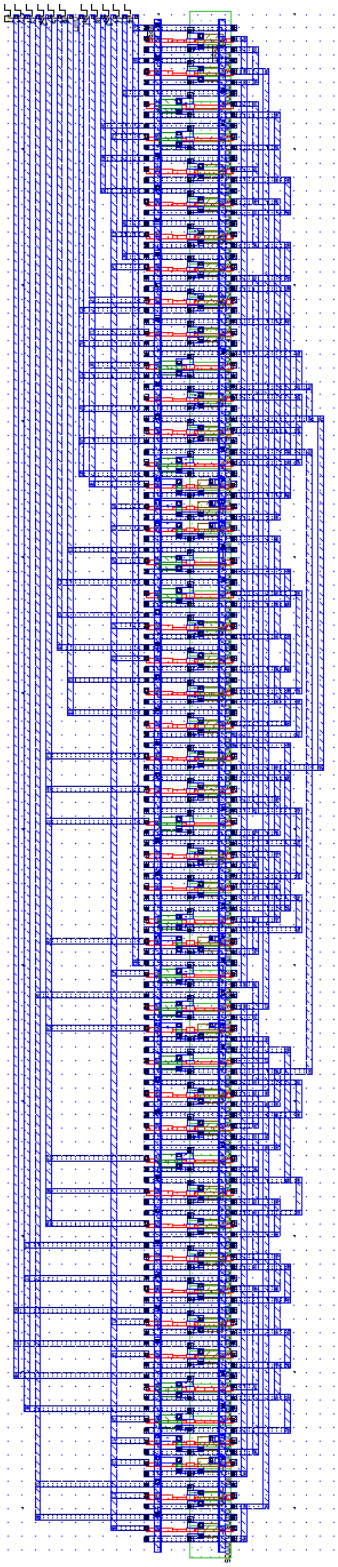

Fig. 4 Layout of an 8-to-1 multiplexer.

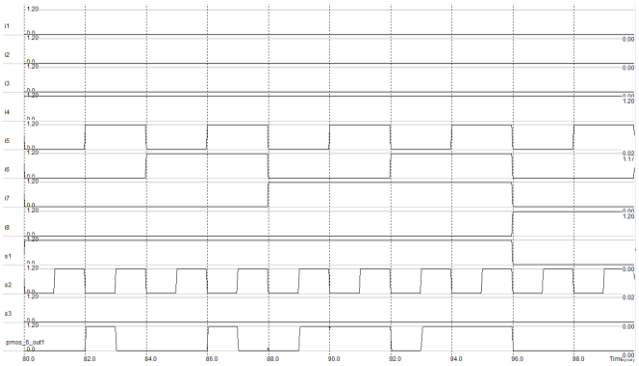

Fig. 5 Timing diagram of an 8-to-1 multiplexer from 80 ns to 100 ns.

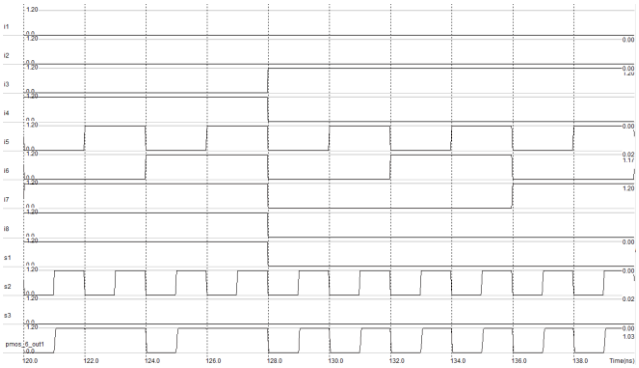

Fig. 6 Timing diagram of an 8-to-1 multiplexer from 120 ns to 140 ns.

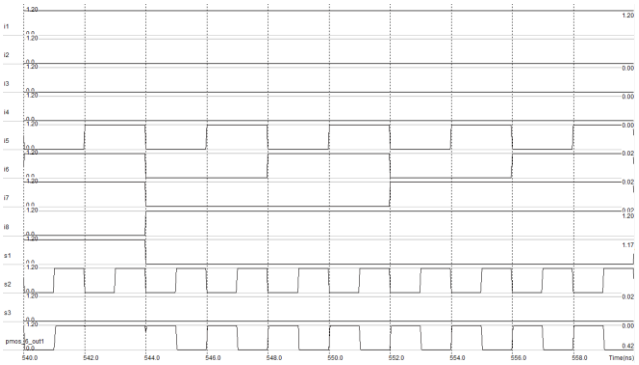

Fig. 7 Timing diagram of an 8-to-1 multiplexer from 540 ns to 560 ns.

IV. Summary

The design and analysis of an 8-to-1 multiplexer has been performed based on the 0.12 µm CMOS transmission gate configuration. Simulations on the transistor-level schematic and layout of the multiplexer have been successfully validated.

References

[1] M. M. Vai, *VLSI Design*, CRC Press, US, 2000.

[2] K. H. Yeap, *Fundamentals of Digital Integrated Circuits Design*, Authorhouse, UK, 2011.

[3] S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, McGraw-Hill, NY, 2005.

[4] K. H. Yeap, J. Y. Lee, W. L. Yeo, H. Nisar, and S. H. Loh, "Design and characterization of a 10 nm FinFET," *Malaysian Journal of Fundamental and Applied Sciences*, vol. 15, pp. 609-612.

[5] K. H. Yeap, M. M. Isa, and S. H. Loh, *Introductory Chapter: Integrated Circuit Chip*, in Integrated Circuits/Microchips, Intech Open, UK, 2020.