Design Optimization of a 4-Bit Synchronous CMOS Counter for High-Speed and Area Efficiency

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Abstract— The objectives of the low power VLSI circuit are to reduce the system's energy footprint and power consumption while enhancing battery life and performance. The scaling architecture, commonly referred to as a counter, adjusts the values of an operator based on its prior state. The counting technique may yield temporal and frequency statistics. The fundamental cause of excessive power consumption in scaling circuits is clock power dissipation during standby. Approximately one-third of a counter's total power consumption is allocated to the clock signal. This research reduces the quantity of switches employed to conserve energy. The counter's minimal power usage is attributable to efforts aimed at alleviating stress on the flip-flops. Integrating TSPCL with SVL (Self-Controllable Voltage Level) is a feasible approach to achieve this objective. TSPCL can perform the Flip-Flop operation swiftly while consuming low power. The SVL approach is more straightforward as it necessitates fewer transistors, resulting in less energy consumption from leakage current. The new model conserves 27% more energy than its predecessor. The suggested method identifies viable functionality for advanced, low-power devices.

Keywords— Low Power, High speed,lower SVL, Upper SVL, modified DFF, Modified XOR gate, 45-nm CMOS.

1. Introduction

In logic circuits, a Flip-Flop is employed to provide a binary output of 0 or 1. Its principal function is archival storage. The flip-flop is unmatched in sequential storage capabilities. In a scalable circuit, the frequency of a process or event can be quantified by introducing a clock signal. It enumerates the pulses received from the input line. It is vital to maintain a reliable, low-energy clock. This reduces the circuit's power consumption. Synchronous and asynchronous counters are utilized in Complementary Metal-Oxide Semiconductor Very Large Scale Integration. The output of one flip-flop (FF) can function as the clock input for the subsequent FF in an asynchronous counter; however, this is unfeasible in a synchronous counter. The propagation time might be reduced by employing a distinctive single-edge-triggered D flip-flop; however, this type of flip-flop is unsuitable for high operating frequencies. A low-power scaling circuit employing priority encoding can condense several binary inputs into a single output. In a quasi-synchronous configuration, energy is expended more rapidly. Scaling circuit for a pseudo-clock. These methods may yield good layouts, but their scalable blueprints are excessively huge. Bi-stable storage components are frequently employed in low-power scaling designs. This paper is organized as follows: Section I is an introduction, Section II is a literature survey, Section III presents an existing method, Section IV presents a proposed method, and Section V presents a conclusion and future scope.

2. literature survey

This study designs a fast binary counter with a short critical path using Cellular Automata (CA). In computer architecture and digital systems, counters—which combine the capabilities of adders and registers—are crucial. Despite their widespread use, counters have performance-impairing constraints. In many binary systems, CA can also function as a trustworthy random number generator. Von Neumann and Elam started studying CA in the 1940s after realizing its potential for simulating intricate systems. According to Encyclopedia Britannica, CA is the "simplest model of a geographically dispersed process" and can depict a variety of systems. John von Neumann and Arthur Burks coined the phrase "self-reproducing automata" to promote additional study. Elam and associates at Los Alamos created recursive geometric patterns in 1967 by using computers to create one-dimensional CA progression. This paper investigates a binary method that enhances CA. This section presents the fundamental components. Implementation issues and relevant literature are covered in Section II. Section IV examines the practical ramifications of flip-flops, whereas Section III presents them. Section V brings the work to a close. Systematic construction, progressive design, and circuit reuse to increase efficiency are important characteristics of a binary counter. Structural flaws may be visible in common layouts. Multiple variations arise when bits toggle for twice as long as the preceding bit. A binary counter often propagates signals over long distances by using logic gates with increasing fan-in at each flip-flop input. Counters reorganize and speed drops as the area grows. To deal with these problems,

delay lines are employed. Delay results from the need to validate lower-order bits before activating higher-order bits. The counter size increases exponentially with each increment in both scenarios.Integrated Circuits (ICs) have become faster and more compact as technology advances. However, this speed increase has a drawback: increased power consumption might cause portable devices' batteries to run out more faster. Leakage electricity becomes a persistent problem when electronics get smaller. Digital integrated circuits are dominated by memory circuits, particularly Static Random Access Memory (SRAM). Advances in Complementary Metal Oxide Semiconductor (CMOS) technology have unlocked the creation of dense, high-performance chips, but these gains often bring increased power demands and rising temperatures. Memory chips continue to be the most widely used CMOS ICs. To address these power hurdles, engineers have crafted innovative strategies to cut SRAM energy use during read and write cycles. Random Access Memory (RAM) is the backbone of electronic design, but the need to drive large capacitances in address, word, and bit lines can push power consumption even higher. Designing effective SRAM is a delicate balancing act: shrinking cell size with smaller transistors, ensuring stable read and write operations, reducing power through lower supply voltages, curbing leakage current, and minimizing voltage swings on bit lines.

3. Existing method

3.1 D FLIP FLOP WITH MODIFIED TSPCL

The True Single Phase Clock (TSPCL) technique is used to implement the flip-flop. The primary objective of TSPCL [1] is to achieve high-speed flip-flop operation. The circuit consists of eleven transistors, with PMOS transistors comprising half of the total. The D Flip-Flop shown in Figure 1 was designed using TSPCL [2]. When D = 0 and CLK is LOW, the N2 transistor is active, which in turn activates the P1 and P2 transistors. P3 then outputs a logic high, which is inverted to produce a logic low. The D input is gradually reversed while maintaining a consistent output.

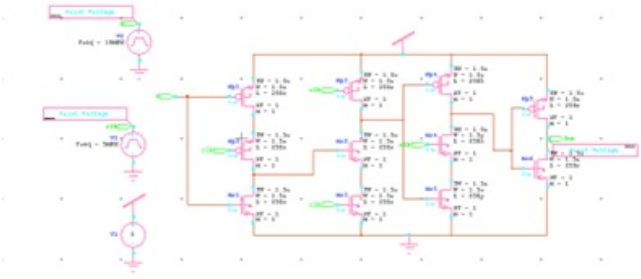

Figure 1: Schematic of Upper SVL

3.2 LOWER SVL

Three transistors—two PMOS and one NMOS—combine to generate the bottom SVL in the figure above. While the NMOS gate is grounded, the PMOS gates receive the input clock. The NMOS is turned off when calk is set to 1. A PMOS conducts electricity when connected to ground. Supply voltage 1 is activated when calk is set to 0. Adjusting the bias can reduce leakage current [2] when the gadget is not in use. The SVL decreases, as Fig. 3 illustrates. This is the most typical implementation of the CMOS D FF circuit [10]. Controlling leakage power is crucial in CMOS technology. When the circuit is off, lowering the supply voltage contributes to power conservation and longer battery life. In the CMOS D FF circuit, the SVL technique reduces signal noise and power consumption [7]. By utilizing fewer transistors, the new design also lowers dynamic power usage.

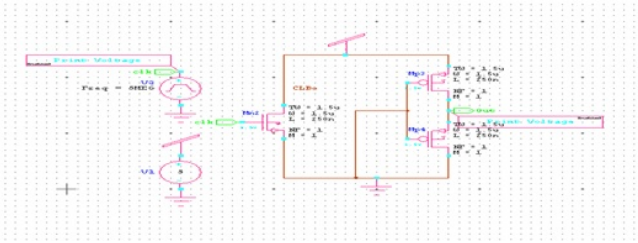

Figure 2: Schematic of Lower SVL

3.3 D FLIP FLOP WITH MODIFIED SVL

Seven PMOS and eight NMOS transistors are among the fifteen carefully placed components shown in the above diagram. While the D flip-flop itself depends on both power and ground to operate, changing the supply voltage level (SVL) momentarily disables N1 and N2 within the flip-flop. Three dynamic states (N1) and two static states (P2) appear in this configuration. With both P1 and N3 switches left open, P2 maintains system functionality while P1 is unavailable. The supply voltage needs to remain between Add and VT in order for N1 and N2 to function as pull-up networks. Static power consumption is greatly reduced when NMOS transistors are connected in series. P2 and P3 form a pull-down network with a small positive voltage instead of connecting directly to ground. In addition to lowering the supply voltage, this series connection of NMOS transistors reduces leakage current during standby. This design reduces dynamic power consumption significantly without compromising performance, despite the fact that leakage power is still a chronic problem because of its dependence on input voltage and current. Figure 4 shows the D flip-flop's improved SVL arrangement.

3.4 DESIGN OF D FLIP- FLOP USING STATIC CMOS

By using dynamic mode static CMOS transistors, the D flip-flop reduces the number of transistors from the usual 20 to

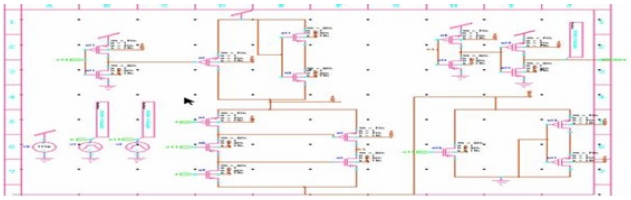

Figure 3: Schematic of Modified D Flip flop using SVL

just five. In addition to saving important semiconductor area, this simplified architecture increases efficiency by over 40% when compared to conventional NAND-based alternatives. As threshold voltage and gate oxide thickness drop, leakage current emerges as the primary cause of power loss in CMOS digital circuits. A compact configuration of three NMOS and two PMOS transistors characterizes the novel D flip-flop architecture.

4. PROPOSED 4 BIT COUNTER DESIGN

4.1 D FLIP FLOP USING 5 TRANSISTORS

For improved performance, this creative design combines D flip-flops with multi-threshold CMOS technology. In a simplified five-transistor D latch, Figure 5.1 depicts the positive edge triggering moment. Transistors N1, N2, and P2 activate when the clock and input signals both spike high, while P1 and N3 remain inactive, resulting in an increasing output. In a single clock cycle, the input quickly moves to the output. This high-speed five-transistor D flip-flop's circuit is shown in Figure 3. P2 and N2 stay off, P1 and N1 are active, and N3 reacts to the low output when the clock is high and the input is low. When the clock and output are both high, P1 moves aside, allowing N1, N2, and P2 to take control while N3 remains passive. The output reacts to a low clock by turning on P1 and turning off N1, N2, P2, and N3. The circuit was rigorously tested using the Tanner EDA tool after the schematic was finalized (see Fig. 1). Matching inputs consistently result in matching outcomes, according to S-Edit simulations.

As seen schematically here, a 5-transistor D flip flop pro-

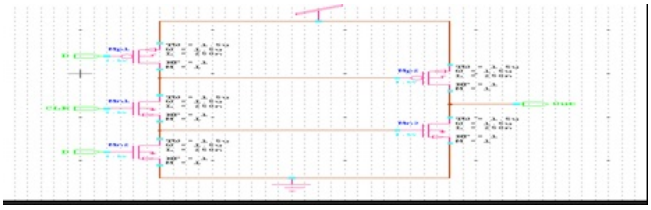

Figure 4: Schematic of D Flip-flop using 5 Transistors

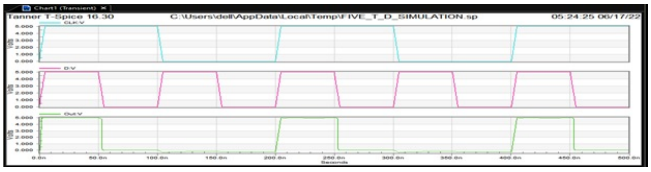

Figure 5: Simualtion of D Flip flop using 5 Transistors

duces a 1 when CLK is high and a 0 when CLK is low.

4.2 Design of XOR Gate Using Pass Transistor

An XOR gate built using pass transistor logic is shown in the diagram. The source and drain terminals of the transistor receive the input in this configuration rather than the gate terminal.Two transistors make up the circuit: one pass transistor uses the B signal as its gate input to propagate the ABAR signal, while the other uses the BBAR signal as its gate input to propagate the A signal. Two transistors have connected outputs.By employing pass transistors to implement an XOR gate, this design reduces the number of transistors from 12, which is necessary for a static XOR gate, to just two [7]. As a result, the circuit uses less power and takes up less space. This XOR gate requires two CMOS inverters and two NMOS transistors.two NMOS transistors. The output of the simulated XOR gate [8] is zero if the logic levels of its two inputs, A and B, are the same, and one if they differ (as seen in the above figure).

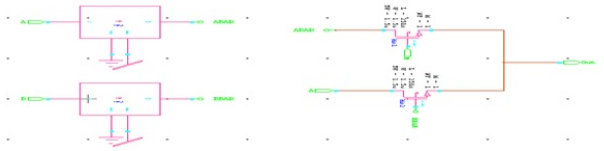

Figure 6: Schematic of XOR gate using 6 Transistors

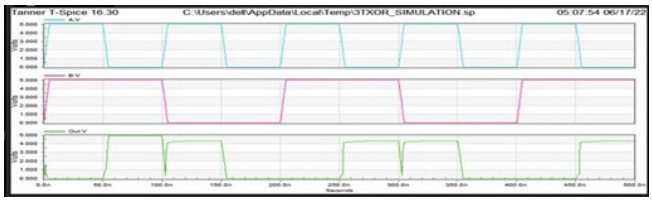

Figure 7: Simulation of XOR gate using 6 Transistors

4.3 PROPOSED COUNTER DESIGN

5. Conclusion

Using four D flip-flops, combinational logic (such as XOR gates), and buffering components, the developed 4-bit synchronous up counter exhibits efficient and reliable sequential logic operation. The counter generates a binary count sequence with a modulus of 16 (MOD-16), ranging from 0000 (0) to 1111 (15).

The circuit eliminates cumulative propagation delays commonly seen in ripple (asynchronous) counters by achieving simultaneous state transitions through the use of a shared clock signal to drive all flip-flops. As a result, the total propagation delay (t_{pd}) of the counter is given by:

$$t_{pd} \approx t_{clk \to Q} + t_{logic} \tag{1}$$

instead of $N \times t_{ff}$ in asynchronous counters.

A higher maximum operating frequency (f_{max}) is therefore achieved:

$$f_{max} \approx \frac{1}{t_{clk \to Q} + t_{logic}} \tag{2}$$

Key Technical Characteristics

- Number of states: 16 (MOD-16)
- Flip-flops required: 4
- Clocking: Common (parallel clock distribution)

- State transition: Synchronous (simultaneous switching)
- Delay: Lower compared to ripple counters
- Speed: Higher due to reduced propagation delay
- Power consumption: Slightly higher due to additional combinational logic
- Hardware complexity: Moderate (requires gating logic for correct counting sequence)

Logic gates, such as XOR gates for toggle conditions, ensure accurate bit transitions based on lower-order outputs, enabling deterministic and error-free counting. The use of buffering and master-slave configurations further enhances timing stability and signal integrity.

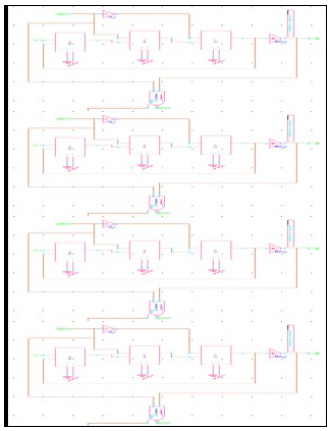

Figure 8: Schematic of Proposed 4 BIT Counter with modified XOR-D Flip-Flop

Overall, the synchronous counter provides high-speed, reliable, and scalable performance, making it suitable for applications such as digital clocks, frequency division, timers, and control systems, where precise timing and synchronization are essential.

6. Conclusion

Using coordinated flip-flop switching and combinational logic, the synchronous counter under analysis exhibits controlled and regulated state transitions. Certain states, such as $QCQBQA = 110$ (decimal 6), activate logic gates (A1, A2) during operation, enabling conditional toggling of successive flip-flops. Flip-flop B toggles based on the applied logic conditions, ensuring proper sequence advancement, while flip-flop A switches from logic 1 to 0 on the falling edge of the clock.

After the ninth clock pulse, the counter resets to a predetermined state ($QCQBQA = 000$), indicating a truncated counting sequence (MOD-9 counter) rather than a full binary cycle. This synchronous reset ensures that all flip-flops return to their initial states simultaneously, thereby preventing glitches and ensuring deterministic operation.

From a timing perspective, the overall propagation delay is given by:

$$t_{pd} \approx t_{clk \to Q} + t_{logic} \tag{3}$$

where:

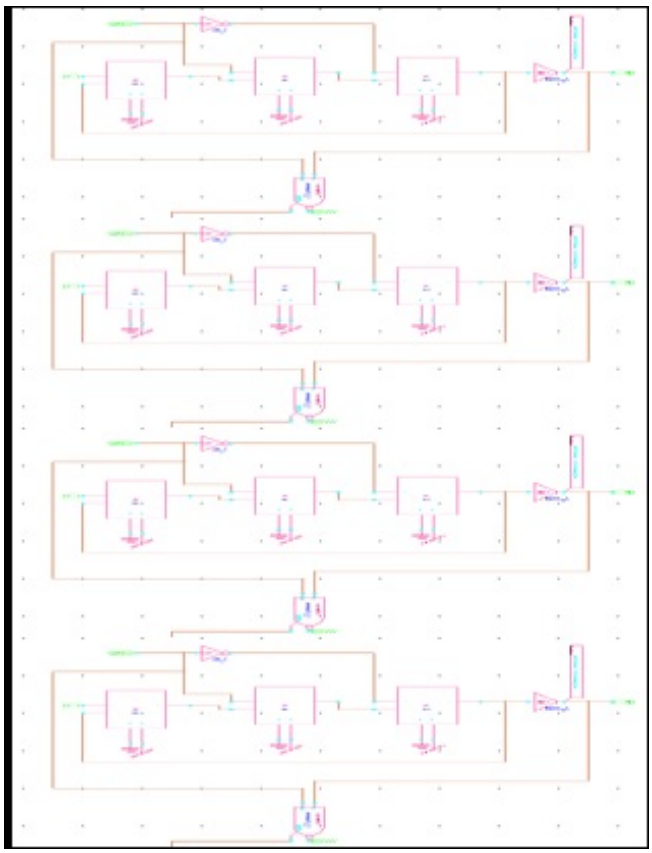

Figure 9: Simulation of Proposed 4 BIT Counter with modified XOR-D Flip-Flop

- $t_{clk \to Q}$ = flip-flop delay
- t_{logic} = delay introduced by combinational logic gates

Unlike asynchronous counters, the delay does not accumulate across stages. Therefore, the maximum operating frequency is:

$$f_{max} \approx \frac{1}{t_{clk \to Q} + t_{logic}} \tag{4}$$

Key Technical Factors

- Counter type: Synchronous truncated counter
- Modulus: MOD-9
- Number of flip-flops: 3 (A, B, C)
- State sequence: $000 \to \cdots \to 110 \to 000$
- Clocking: Common clock (parallel triggering)
- Reset mechanism: Synchronous reset at count = 9
- Propagation delay: Single-stage (non-cumulative)
- Speed: High (supports high-frequency clock operation)
- Reliability: High due to simultaneous reset of all flip-flops

Although each flip-flop and logic gate introduces finite delay, the synchronous architecture minimizes timing errors and enables operation at higher clock frequencies compared to ripple counters. Ensuring simultaneous reset of all flip-flops is critical, as improper reset timing may lead to invalid states.

Overall, the counter delivers high-speed, stable, and predictable performance, making it suitable for applications such as frequency division, sequence generation, and digital control systems, particularly where non-standard counting sequences (e.g., MOD-9) are required.

Table 1: Comparison of Existing and Proposed Technology

S.No	Parameter	Existing (250nm)	Proposed (16nm)
1	Area	184 Transistors	76 Transistors
2	Power	4.68 W	0.01102 W
3	Delay	10.2946 ns	90 ps

7. conclusion and future scope

T-Shoe Sandal T Flip flips, USVL, and LSVL are the methods used to construct the current counter. The proposed method creates a simultaneous counter with lower power consumption, while clock gating increases both power and space needs. The clock in this configuration needs flip-flops in order to change time zones. This resolves the circuit's complexity issue. Pass transistor technology simplifies circuits by eliminating superfluous transistors and lowering the power output of leakage current. The new design results in a 46.8% reduction in energy use. The suggested approach finds practical uses for state-of-the-art, low-power technologies.Since the suggested strategy allows us to utilize fewer transistors overall, it is beneficial in situations when minimizing power consumption is of the highest significance.

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